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EXAMINER	
TODD, GREGORY G	

ART UNIT	PAPER NUMBER
2157	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/885,290	MARKSON ET AL.	
	Examiner	Art Unit	
	Gregory G. Todd	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,8,10-12,15,40-43,45-47,49-53,55-57 and 59-68* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,8,10-12,15,40-43,45-47,49-53,55-57 and 59-68* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's amendment filed, 14 August 2007, of application filed, with the above serial number, on 19 June 2001 in which claims 1, 40, 50, 60, 63, and 66 have been amended. Claims 1-2, 7-8, 10-12, 15, 40-43, 45-47, 49-53, 55-57, and 59-68 are therefore pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 7-8, 10, 15, 40-43, 45, 49-53, 55, and 59-68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau et al (hereinafter "Blumenau", 6,421,711) in view of DeMoss et al (hereinafter "DeMoss", 5,778,411).

As per Claim 1, Blumenau teaches a computer-implemented method of allocating storage to a host processor comprising:

a control processor receiving a request to allocate storage to the host processor (at least col. 31, lines 27-39; col. 33, lines 29-66; host requesting allocation of a volume); and

the control processor associating one or more logical units from among one or more storage units to the host processor by (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN):

the control processor configuring a gateway device to map the one or more logical units to the host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the one or more storage units to give the host processor access to the one or more logical units (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the host processor accesses the one or more logical units, which are associated with the host processor by the control processor (at least col. 9:18-57; col. 32:13-31; LUNs connected to hosts with gatekeeper volume).

Blumenau fails to explicitly teach the gateway device being a physical device and separate from the control processor, without the host processor knowing which of the one or more logical units from among the one or more storage units are associated with the host processor. However, the use and advantages for using such a system is well known to one skilled in the art at the time the invention was made as evidenced by the teachings of DeMoss. DeMoss teaches separate host systems and virtual storage controller wherein physical storage is hidden from the hosts and the host accessing the virtual location (at least Fig. 1, 3; col. 1:54-col. 2:3; col. 6:45-65). All of the component

parts are known in Blumenau and DeMoss. The only difference is using a separate device for such 'virtualization'. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, as all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results.

As per Claim 2. A method as recited in claim 1, wherein:

the control processor configuring the gateway device and the control processor configuring the one or more storage units are performed by the control processor without modification to an operating system of the host processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50);

the gateway device is included in a virtual storage layer (at least col. 32 line 13 - col. 33 line 17; storage subsystem volume / LUN);

the host processor and the one or more storage units are included in a virtual server farm (at least col. 21 line 16 - col. 22 line 63; col. 7, lines 51-65; collection of servers);

the control processor is coupled through one or more storage networks to a plurality of storage gateways that includes the gateway device (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4; storage volumes); and

the plurality of storage gateways are coupled through the storage networks to the one ore more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4).

As per Claim 7. A method as recited in claim 1, further comprising:

the control processor causing the storage of first information that associates processors to logical units (at least col. 21 line 16 - col. 22 line 21; host to LUN to logical volume);

the control processor causing the storage of second information that associates logical units to storage units (at least col. 21 line 16 - col. 22 line 21; host to LUN to logical volume); and

the control processor associating the one or more logical units from among the one or more storage units to the host processor further comprises the control processor mapping the one or more logical units from among the one or more storage units to a boot port of the host processor by reconfiguring the gateway device to logically couple the one or more logical units to the boot port based on the stored first information and the stored second information (at least col. 32 line 13 - col. 33 line 17; boot from storage subsystem volume);

the control processor identifying one or more logical unit numbers corresponding to the one or more logical units (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57; col. 21, lines 16-55);

control processor instructing the gateway device to map the one or more logical unit numbers to the small computer system interface port zero of the host processor based on a unique processor identifier (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57); and

the control processor instructing the one or more storage units to give the host processor having the unique host identifier access to the one or more logical unit numbers (at least col. 31, lines 9-51).

As per Claim 8. A method as recited in claim 1, wherein the request to allocate storage to the host processor is a first request to allocate storage to the host processor, and the method further comprises:

based on the first request, the control processor generating a second request to allocate storage to the host processor (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12);

wherein the control processor is communicatively coupled to a control database (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database);

wherein the second request is directed from the control processor to a storage manager (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database);

wherein the storage manager is communicatively coupled to the control processor, the control database, and a storage network that includes the gateway device (at least col. 11, lines 3-30; Fig. 1; col. 31, lines 9-61; col. 29 line 58 - col. 30 line 12; gatekeeper with configuration database); and

the method further comprises the control processor causing the storage manager to issue instructions to the one or more storage units to give the host processor access to the one or more logical units (at least col. 31, lines 9-51)

As per Claim 10. A method as recited in claim 1, wherein the request to allocate storage specifies a first amount of storage (eg. a single logical volume; see col. 1, lines 40-58) , and wherein the control processor associating the one or more logical units further comprises:

the control processor identifying the one or more logical units of the one or more storage units that, when combined, have a second amount of storage that is at least as great as the first amount of storage specified in the request (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57).

As per Claim 15. A method as recited in claim 1, wherein:

the one or more logical units associated with the host processor include at least a first logical unit from a first volume of a fist storage unit of the one or more storage units and at least a second logical unit from a second volume of a second storage unit of the one or more storage units (at least Fig. 19; col. 21, lines 16-67);

the request to allocate storage specifies a parameter selected from the group consisting of an amount of storage to be allocated and a type of storage to be allocated (at least col. 31 line 9 - col. 32 line 12; col. 6 line 64 - col. 7 line 65; col. 9, lines 44-57; col. 32, lines 58-67; col. 34, lines 2-17).

the control processor is separate from the gateway device, the host processor, and the one or more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4); and

the gateway device is separate from the control processor, the host processor, and the one or more storage units (at least col. 31, lines 9-51; col. 9, lines 18-43; Fig. 1-4).

As per Claim 60. Blumenau teaches restricting volumes 'seen' by the host processors (col. 11:57-12:31), but fails to explicitly teach wherein the host processor does not determine which one or more logical units are associated with the host processor. However, the use and advantages for using such a system is well known to one skilled in the art at the time the invention was made as evidenced by the teachings of DeMoss. DeMoss teaches separate host systems and virtual storage controller wherein physical storage is hidden from the hosts and the host accessing the virtual location (at least Fig. 1, 3; col. 1:54-col. 2:3; col. 6:45-65). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, as all the claimed elements were known in the prior art and one skilled in the art could have

combined the elements as claimed by known methods with no change in their respective functions, and the combination would have yielded predictable results.

As per Claim 61. A method as recited in Claim 1, wherein:

the one or more logical units are associated with one or more logical unit numbers (at least col. 32 line 13 - col. 34 line 59; col. 9, lines 44-57; col. 21, lines 16-55); and

the host processor does not know the one or more logical unit numbers for the one or more logical units that are associated with the host processor (at least col. 11 line 57 – col. 12 line 31; restrict volumes seen by any one host).

As per Claim 62. A method as recited in Claim 1, wherein:

the host processor is a first host processor (at least Fig. 1-3);

the one or more logical units include a first logical unit and a second logical unit (at least Fig. 1-3);

the one or more storage units include a first storage unit and a second storage unit (at least Fig. 1-3);

the first logical unit is associated with the first storage unit (at least Fig. 1-3);

the second logical unit is associated with the second storage unit (at least Fig. 1-3);

the control processor associates the first logical unit and the second logical unit to the first host processor at a first time (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 50; allocated and assigning LUN); and

the method further comprises:

at a second time that is after the first time, the control processor associating the second logical unit with a second host processor by:

the control processor configuring the gateway device to map the second logical unit to the second host processor instead of the first host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the second storage unit to give the second host processor access to the second logical unit instead of the first host processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the second host processor does not determine that the second logical unit is associated with the second host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it);

wherein the first logical unit remains associated with the first host processor (at least Fig. 1-3);

at a third time that is after the second time, the control processor associating the second logical unit with the first host processor by:

the control processor configuring the gateway device to map the second logical unit to the first host processor instead of the second host processor (at least col. 32 line 13 - col. 33 line 17; allocated and assigning LUN, the control processor being a part of the gateway device/gatekeeper and configuring itself);

the control processor configuring the second storage unit to give the fist host processor access to the second logical unit instead of the second host processor (at least col. 31, lines 9-51; col. 33 line 53 - col. 34 line 39; host or host controller having ability to access volumes);

wherein the first host processor does not determine that the second logical unit is associated with the first host processor (at least col. 32, lines 13-43; host obtaining LUNs associated with it); and

wherein the first logical unit remains associated with the first host processor (at least Fig. 1-3).

Claims 40-43, 45, 49-53, 55, 59, and 63-68 do not substantially add or define any additional limitations over claims 1, 2, 7-8, 10, 15, and 60-62 and therefore are rejected for similar reasons.

4. Claims 11-12, 46-47, and 56-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blumenau in view of DeMoss, and further in view of Ofer et al (hereinafter "Ofer", 6,260,109).

As per Claim 11. A method as recited in claim 1, wherein the request is a first request, and the control processor associating the one or more logical units further comprises:

the control processor issuing a second request to allocate one or more volumes on one of the one or more storage units (at least col. 31, lines 27-39; col. 33 line 29 - col. 34 line 50);

the control processor causing the volume to be configured for use with the host processor (at least col. 31, lines 9-51);

the control processor issuing first instructions to the one or more storage units to bind the host processor to the volume by giving the host processor access to the volume (at least col. 33 line 29 - col. 34 line 50);

the control processor issuing second instructions to the gateway device to bind the volume to the host processor (at least col. 33 line 29 - col. 34 line 50; eg. gatekeeper).

Blumenau and DeMoss fail to explicitly teach the volume being concatenated. However, the use and advantages for using such concatenation is well known to one skilled in the art at the time the invention was made as evidenced by the teachings of Ofer (at least Abstract). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate Ofer's use of concatenation into Blumenau and DeMoss' system as this would enhance Blumenau and DeMoss' RAID arrays and subsequently allocated logical volumes to be combined together as this is well known in the art in expanding storage.

As per Claim 12. A method as recited in claim 11, further comprising:

the control processor determining that the second instructions have failed to bind the concatenated volume to the host processor (at least col. 33 line 29 - col. 34 line 50);

the control processor issuing third instructions to the one or more storage units to un-bind the host processor from the concatenated volume (at least col. 33 line 29 - col. 34 line 50; removing and deallocating);

the control processor determining that the first instructions have failed to bind the host processor to the volume (at least col. 33 line 29 - col. 34 line 50); and

the control processor issuing fourth instructions to the one or more storage units to break the volume (at least col. 33 line 29 - col. 34 line 50).

Claims 46, 47 and 56-57 do not substantially add or define any additional limitations over claims 11-12 and therefore are rejected for similar reasons.

Response to Arguments

5. Applicant's arguments with respect to claims 1-2, 7-8, 10-12, 15, 40-43, 45-47, 49-53, 55-57, and 59-68, have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Newly cited Munroe et al, Maffezzoni et al, and Emerson et al (see col. 4:30-44), in addition to previously cited Aziz, Pothapragada et al, Sheets et al, Blickenstaff et al, Aziz et al, Denning et al, Nguyen et al, Nolan et al ('526, '278), Popelka et al, Hickman et al, Tamer et al, and Blumenau '442 are cited for disclosing pertinent information related to the claimed invention. Applicants are requested to consider the prior art reference for relevant teachings when responding to this office action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory G. Todd whose telephone number is (571)272-4011. The examiner can normally be reached on Monday - Friday 9:00am-6:00pm w/ first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on (571)272-4001. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Gregory Todd

Patent Examiner

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SUPERVISORY PATENT EXAMINER